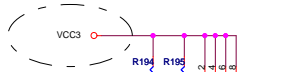


Del R160,R193,R264  
R265: 49.9 -> 100  
R248: 100 -> 169

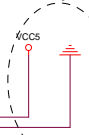
Elitegroup Computer Systems			
Title			
CPU2 (PWR_GND)			
Size	Document Number	Rev	
C	P4M800PRO-M	1.0	
Date:	Thursday, November 17, 2005	Sheet	2 of 30



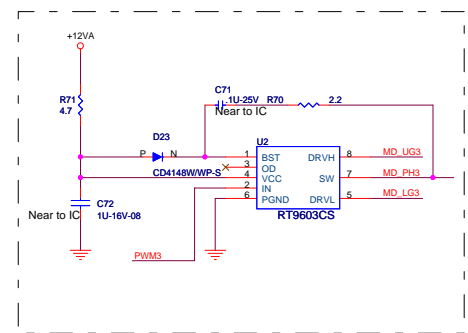
Change VCC12 to VCC3



Disable fourthly Phase.

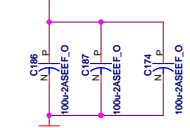


拉回的點斷從4PHASE 中約等長路徑

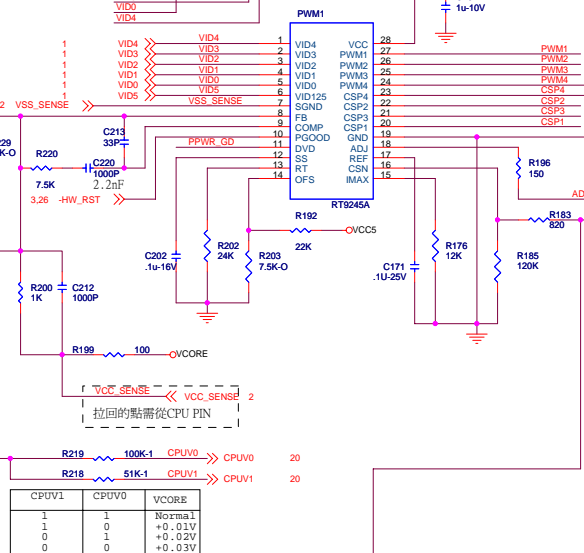


CPU Vcore be modified from 4 phase to 3 phase (05/10/11)  
RT9602CS be changed to RT9603CS

Close to CPU

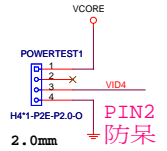


Put CPU component side x3

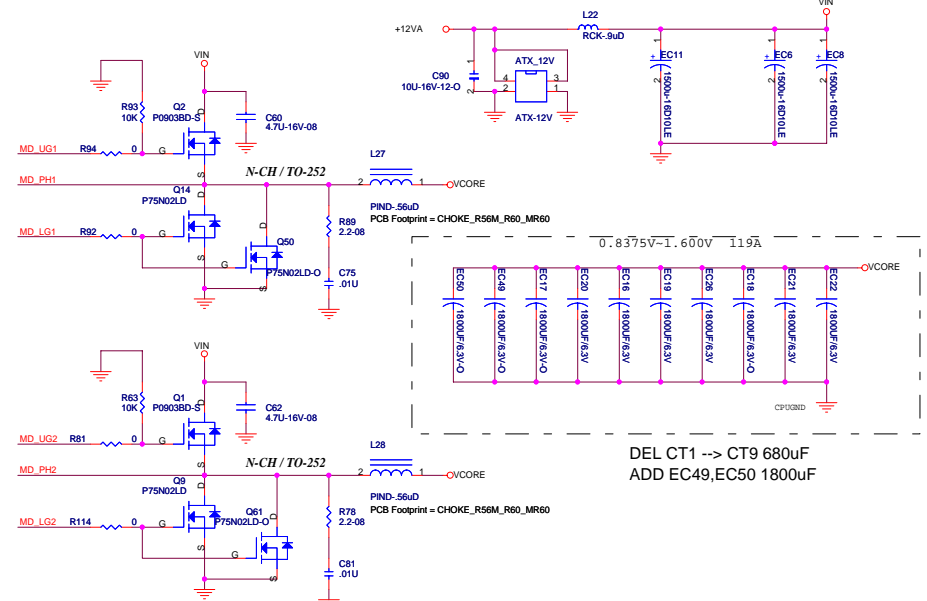
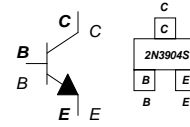


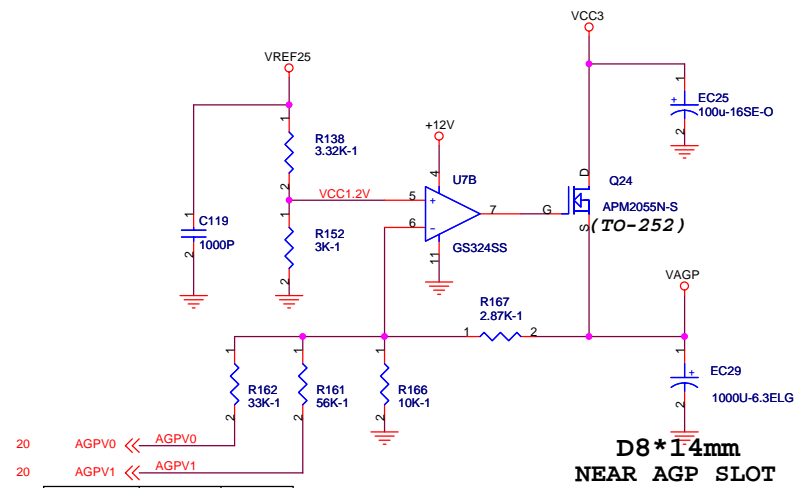
Capacitors change to X7R

置於IC附近,長度500mils以內  
MD\_PH & VCCP CHOKE PIN 拉回走平行線



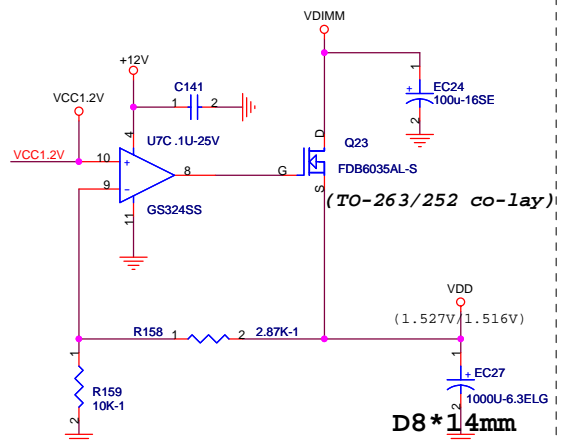
For 04A(78A): 上-(9m)下-(6m)  
For 04B(119A): 上-(9m)下-(6m)  
For 05A(100A): 上-(9m)下-(6m)  
For 05B(125A): 上-(9m)下-(6m)



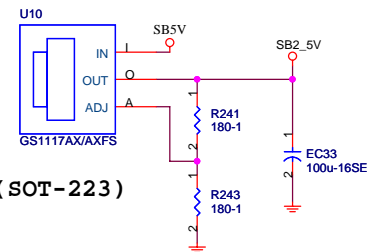
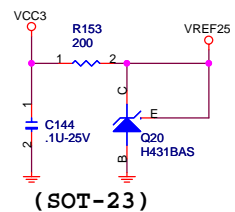
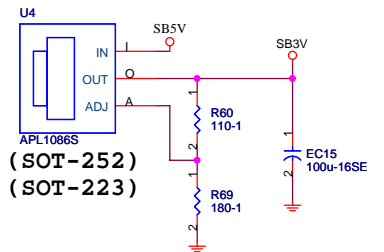
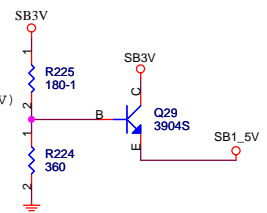
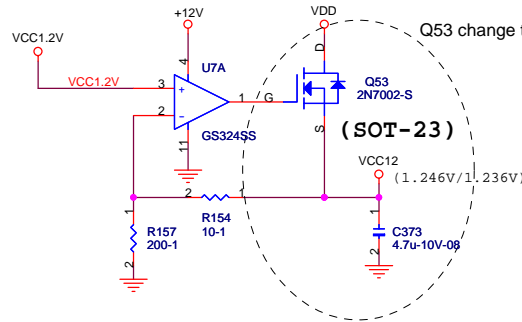
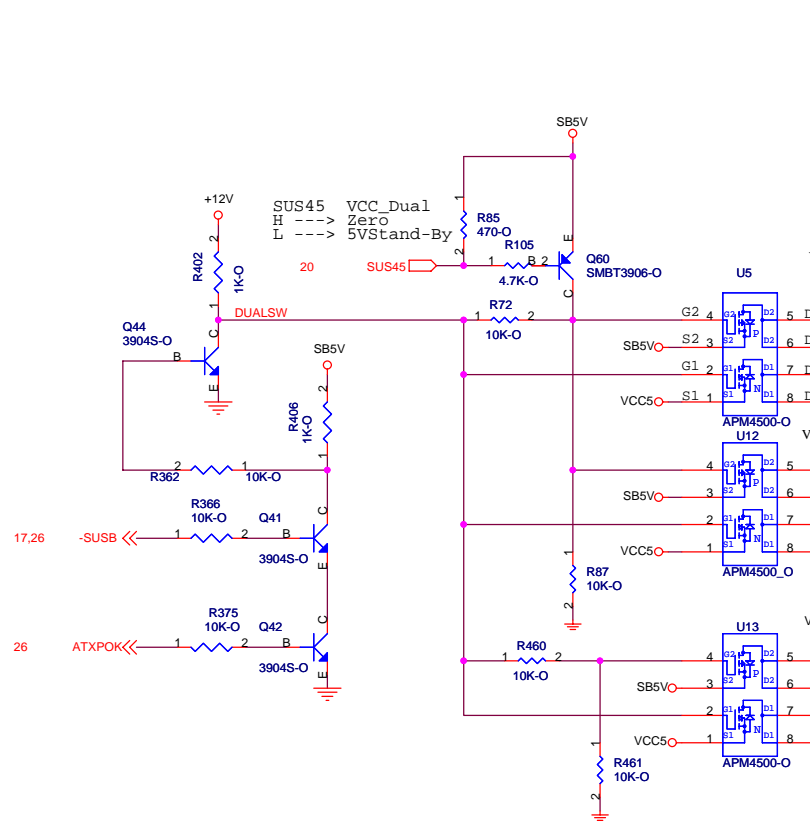
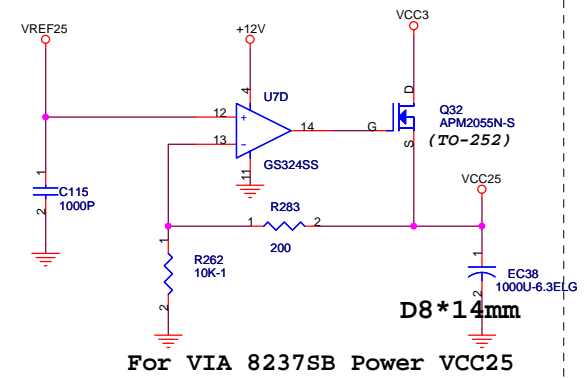


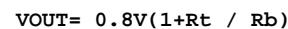
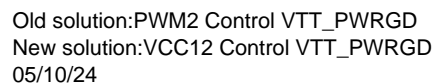
AGPV1	AGPV0	VCORE
1	1	Normal
0	0	+0.05V
1	1	+0.1V
0	0	+0.15V

**For AGP Power VDDQ**



**For VIA P4M800pro VDD Power 1.5V**

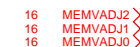




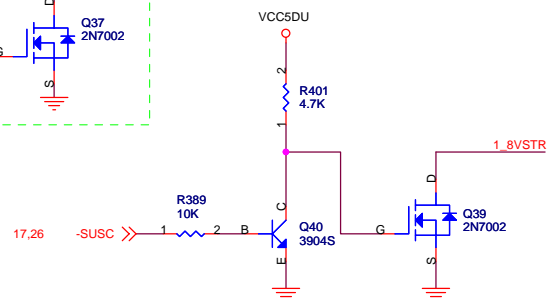
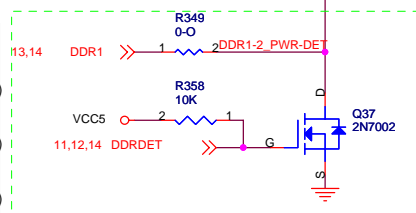
R15: OPEN=1.8V, LOW=2.5V

R15 => Low=2.5V ( DDR2\_DET\_L = Floating ) , If don't install DDR1 & DDR2 .

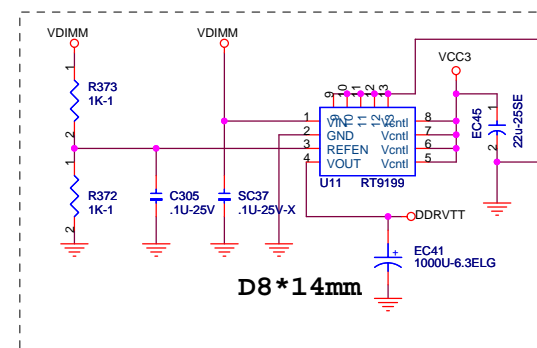
R15 => Open=1.8V ( DDR2\_DET\_L = Low ) , If install DDR1 & DDR2 at the same time .



MEMV2	MEMV1	MEMV0	DDR Vlotage
1	1	1	+0.35V(350mV)
1	1	0	+0.3V(300mV)
1	0	1	+0.25V(250mV)
1	0	0	+0.2V(200mV)
0	1	1	+0.15V(150mV)
0	1	0	+0.1V(100mV)
0	0	1	+0.05V(50mV)
0	0	0	Normal (1.8V or 2.5v)



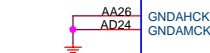
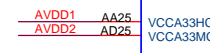
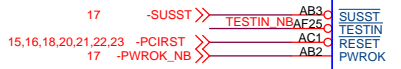
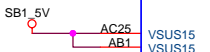
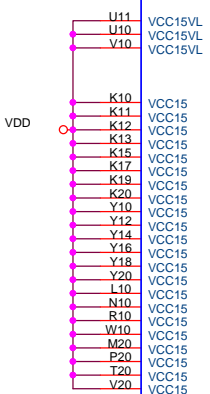
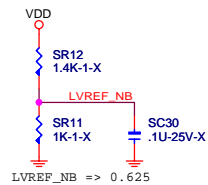
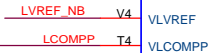
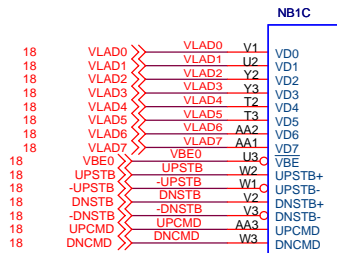
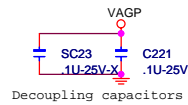
For S5 Disable VDIMM



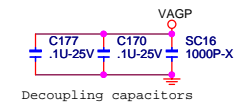
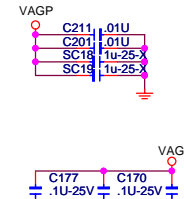
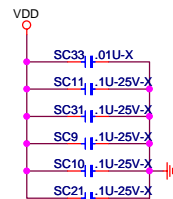
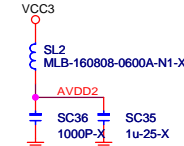
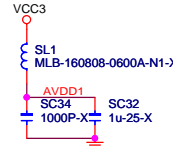
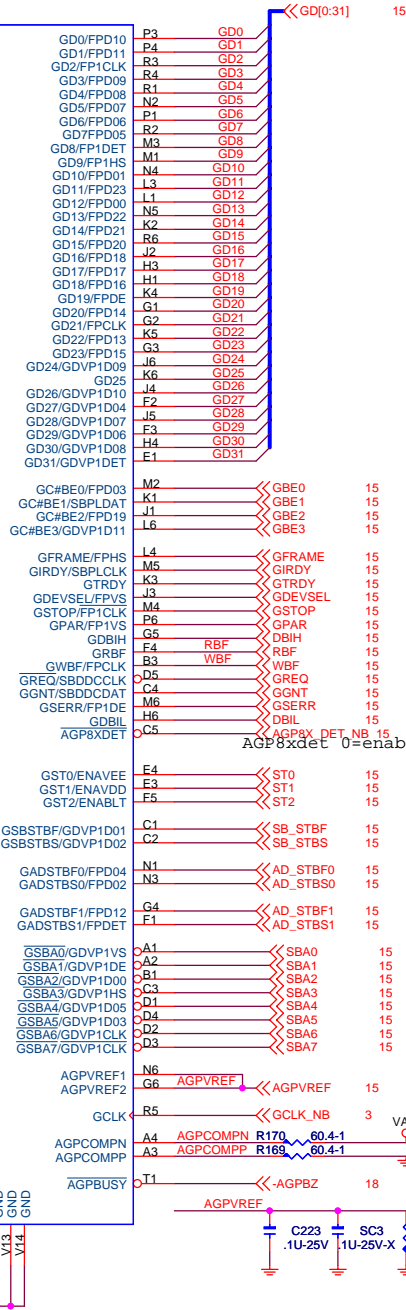




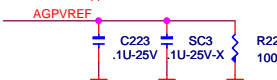




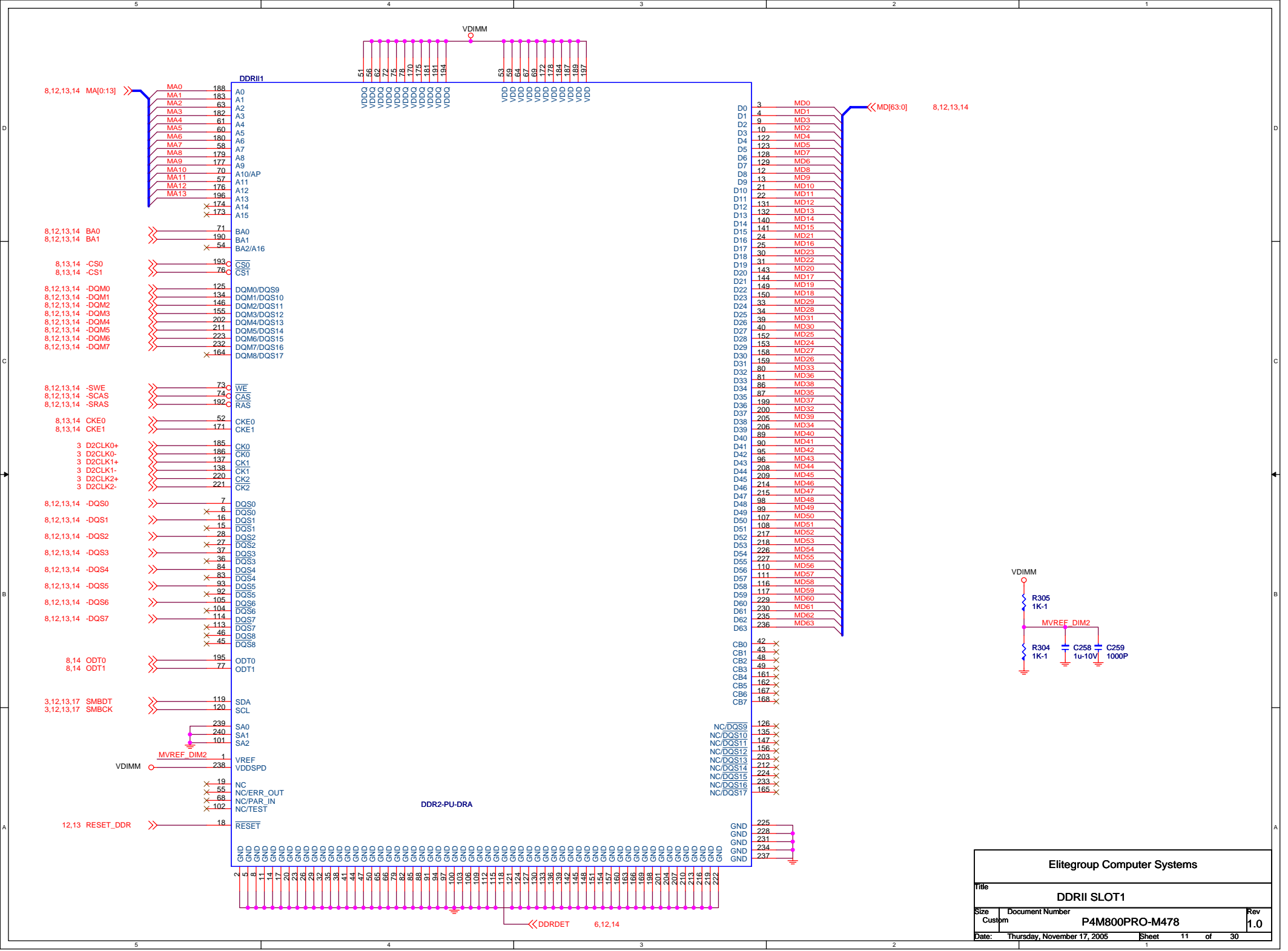
P4M800PROCD-A1

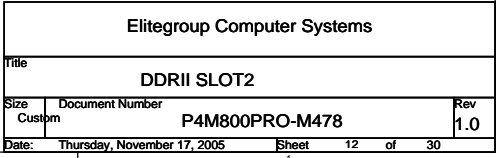


Strapping For NB\_TEST Mode  
TESTIN RBF WBF  
1 x x Disable all TEST mode

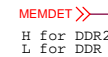
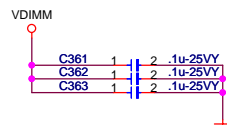


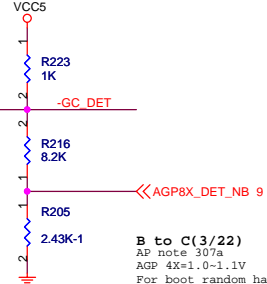
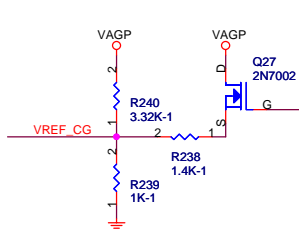
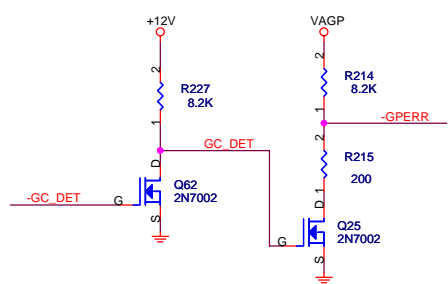
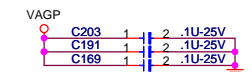
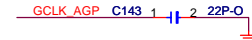
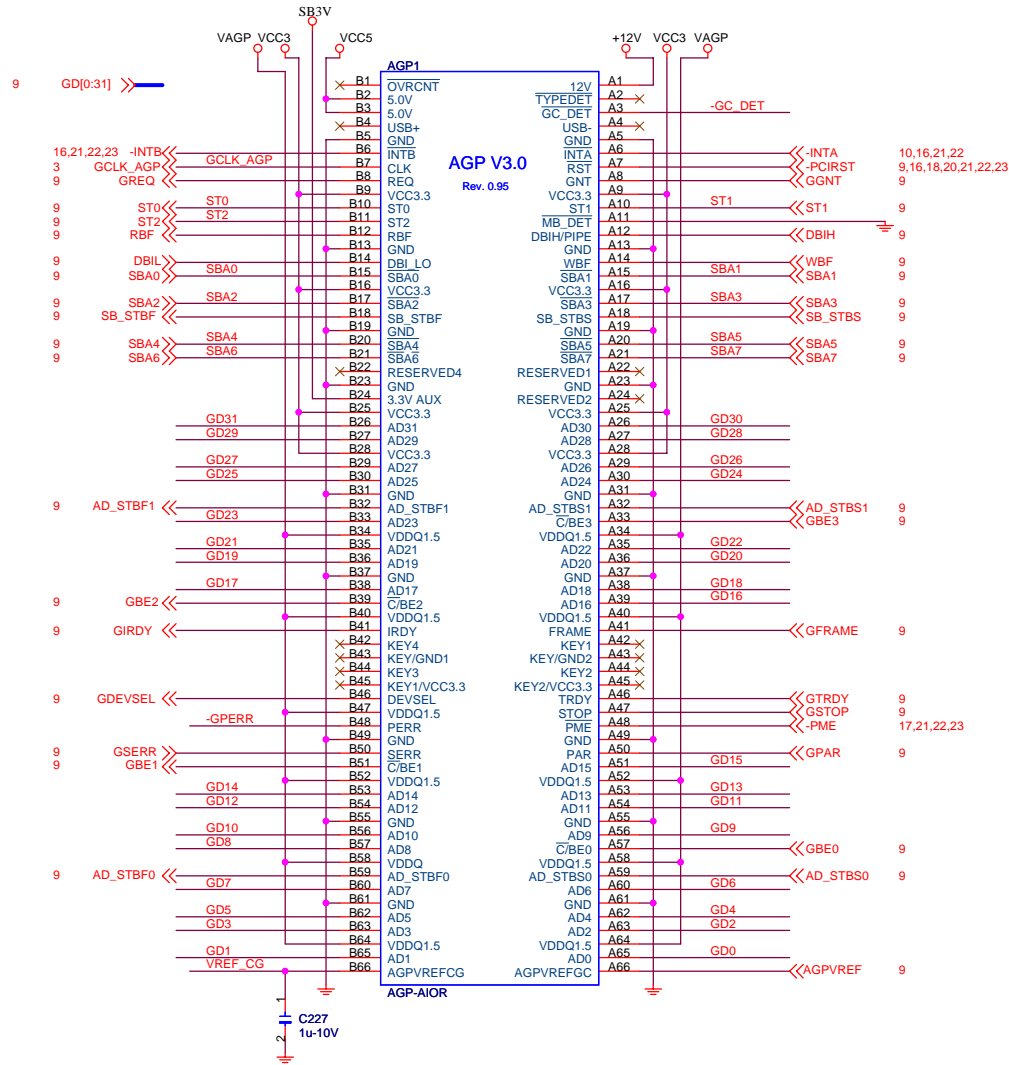




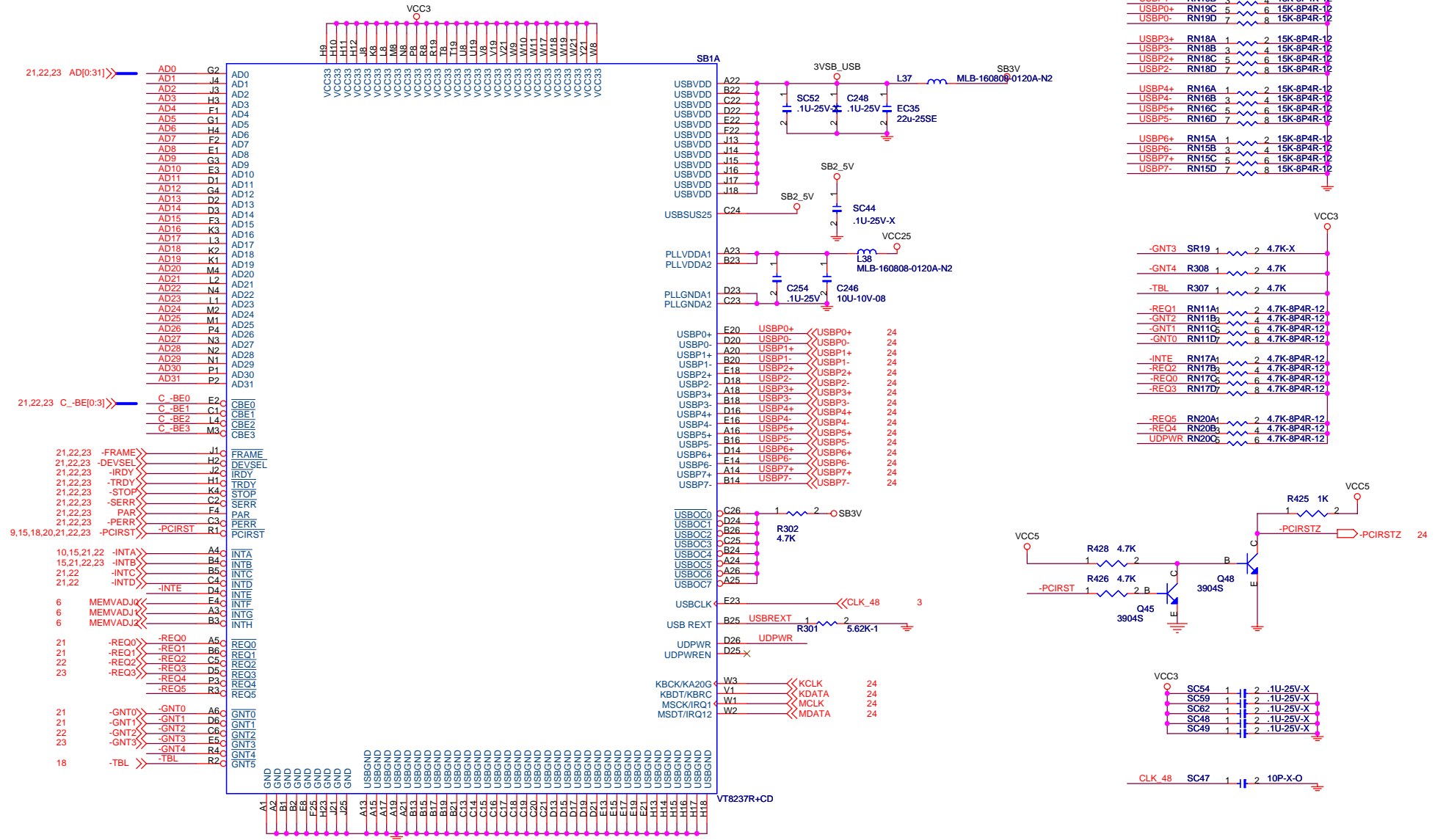




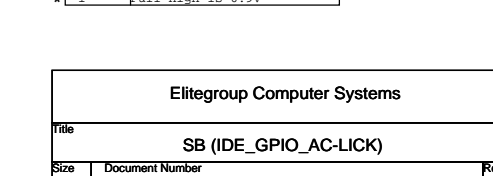
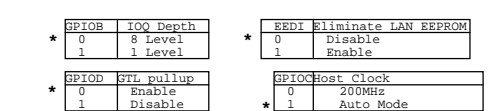
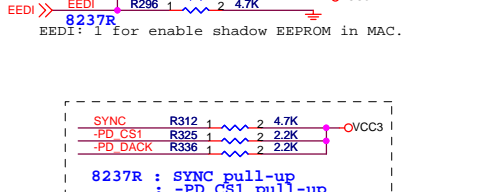
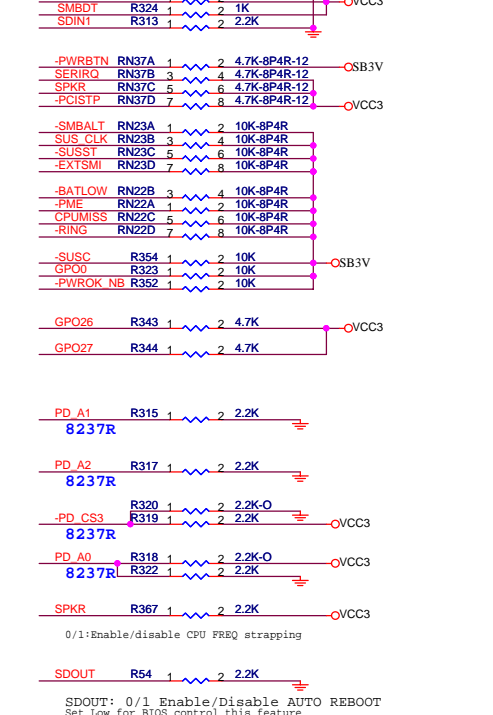
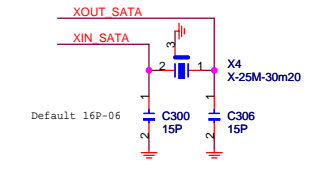
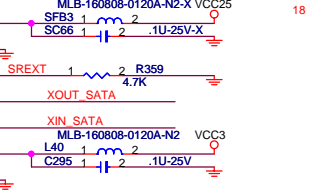
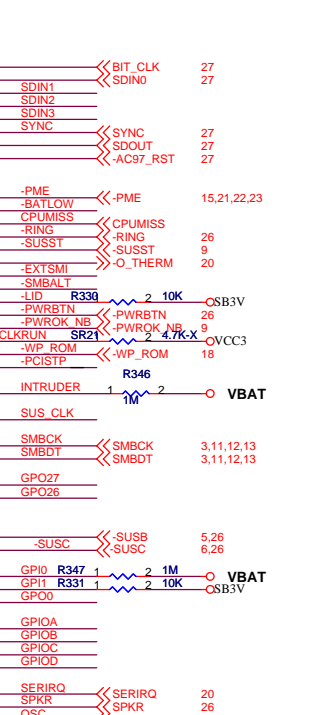
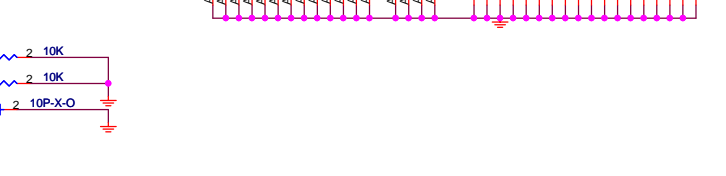
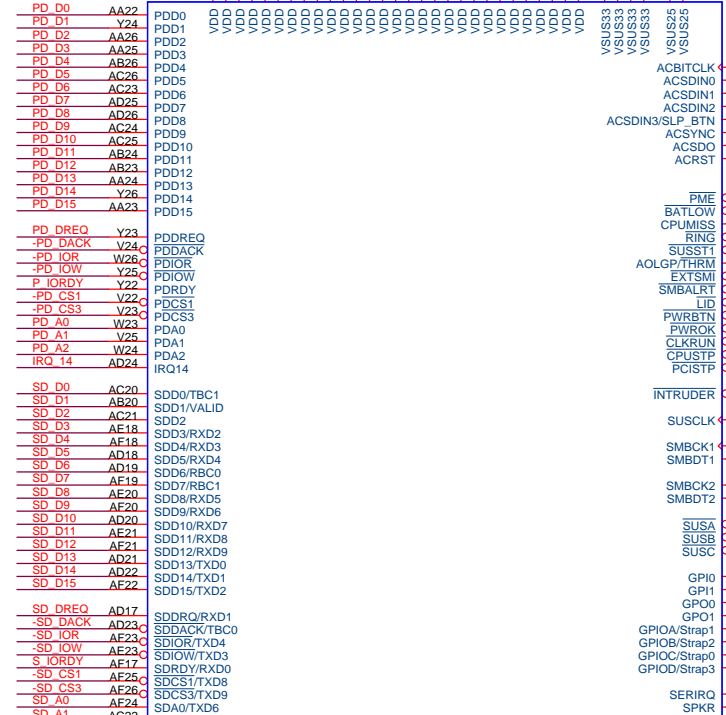
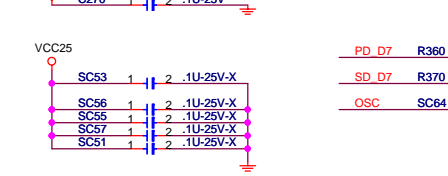
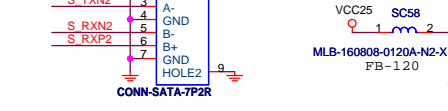
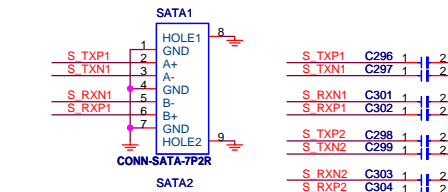
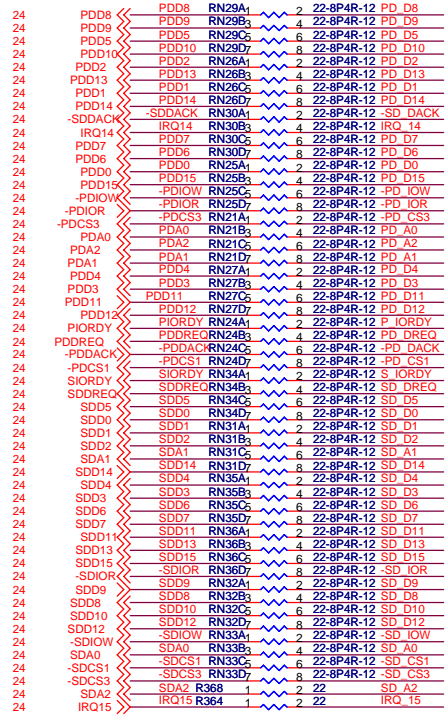


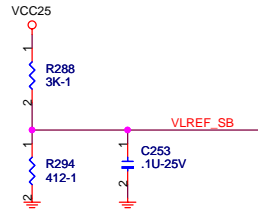


B to C(3/22)  
AP note 307a  
AGP 4X=1.0~1.1V  
For boot random hang \*25\*





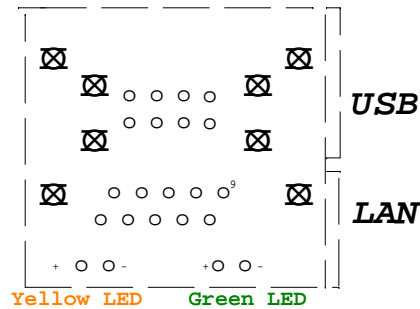




AP note 305: VLREF = 0.3

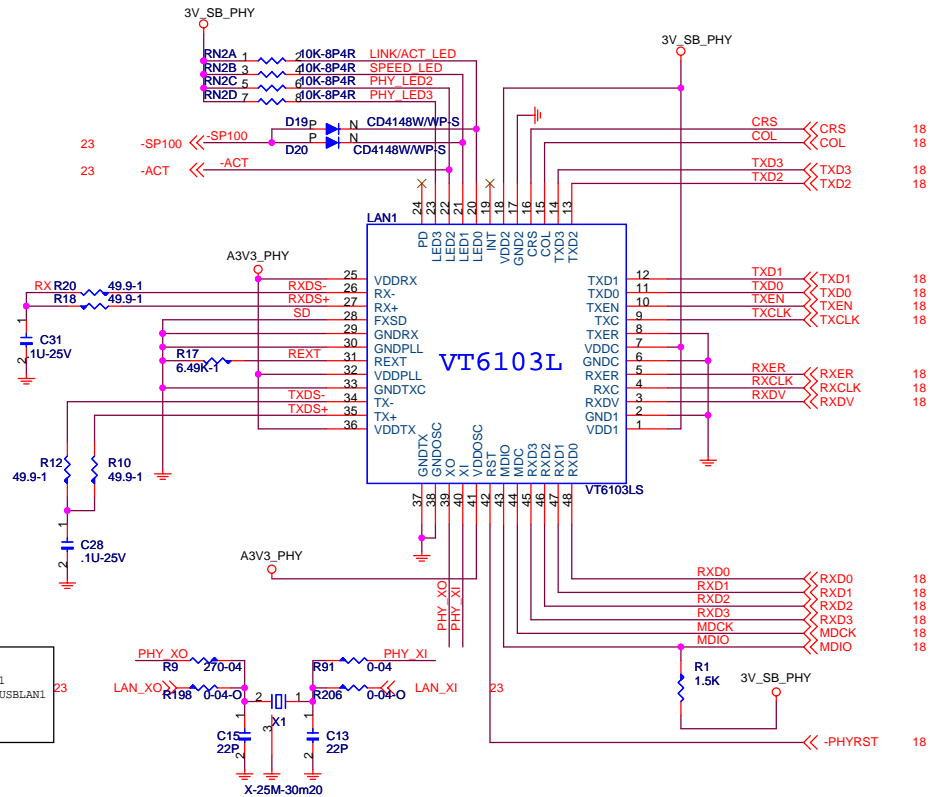
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Title			
SB (VLINK_LPC_MII)			
Size	Document Number		Rev
Custom	P4M800PRO-M478		1.0
Date:	Thursday, November 17, 2005	Sheet	18 of 30

CONNECTOR Solder Side View

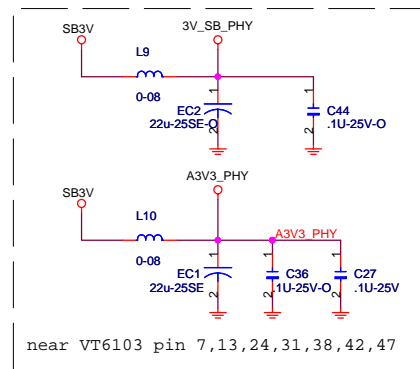


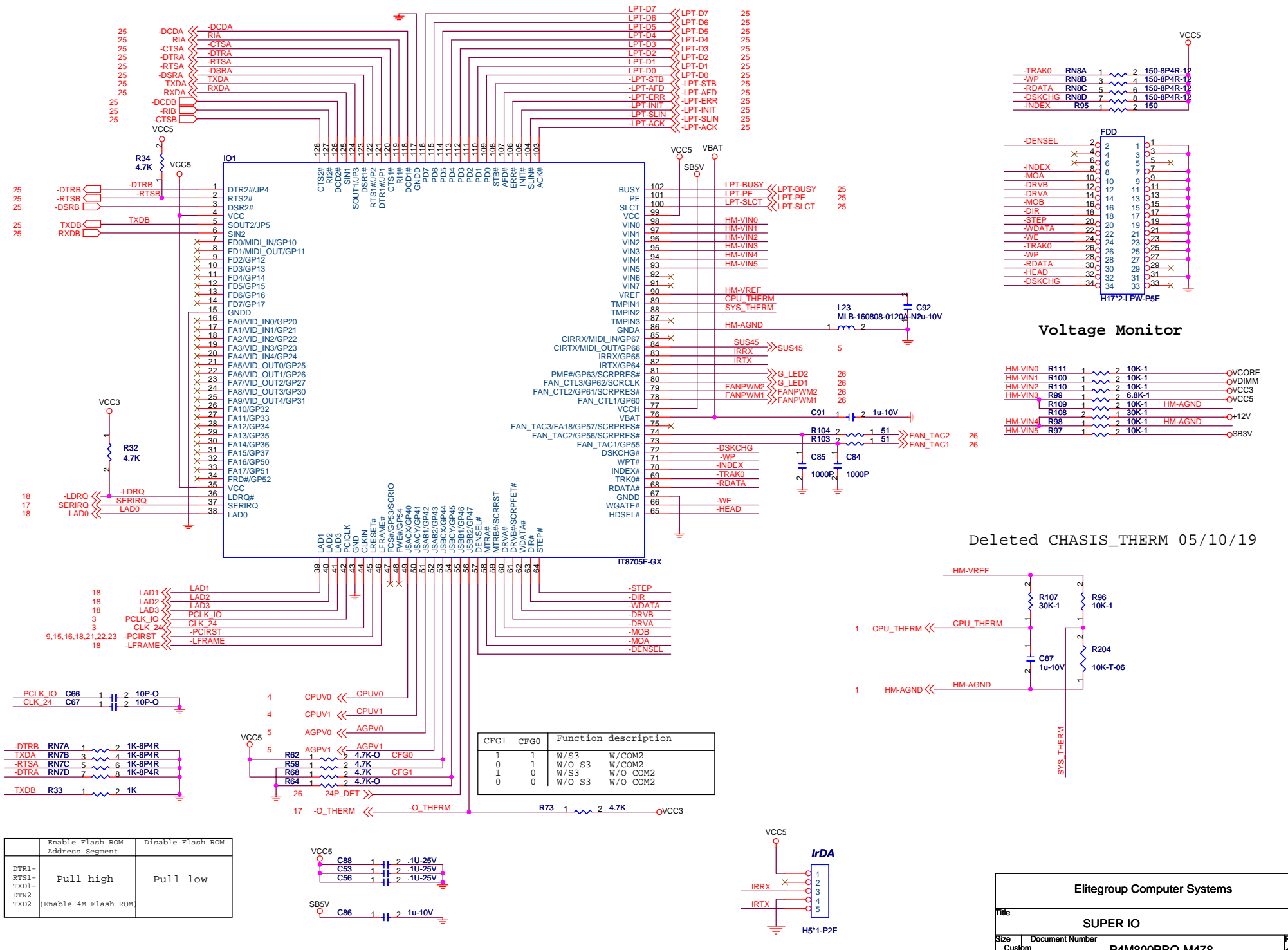
LNA CONN WITH TRSFORM  
LED L-Y / R-G

CONN.USB DUAL PORT+LAN.22P  
90D.W/LED(LY-RG/O).10/100  
TRANS LJ-H51SU3-52.LANKOM.



	LED0	LED1	LED2	LED3	
00	LINK/ACT	SPEED	DUPLEX	COL	
01	PWR/TXACT	LINK/RXACT	SPEED	DUPLEX	
10	SPEED100	SPEED10	ACT	DUPLEX	DEFAULT
11	PWR/TXACT	LINK/RXACT	SPEED	COL	





	Enable Flash ROM Address Segment	Disable Flash ROM Address Segment
DTR1- RTS1- TXD1- DTR2 TXD2	Pull high	Pull low
	(Enable 4M Flash ROM	

CFG1	CFG0	Function description	
1	1	W/S3	W/COM2
1	0	W/O S3	W/COM2
0	1	W/S3	W/O COM2
0	0	W/O S3	W/O COM2

Elitegroup Computer Systems

Title

SUPER IO

Size

Custom

Document Number

P4M800PRO-M478

Rev

1.0

Date

Thursday, November 17, 2005

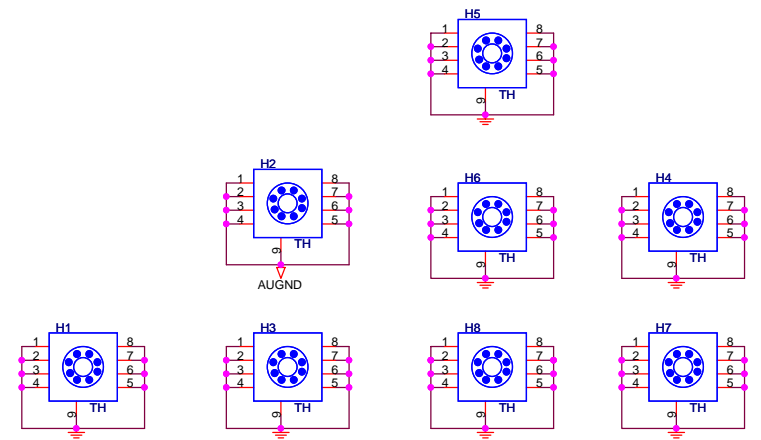
Sheet

20

of

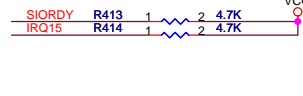
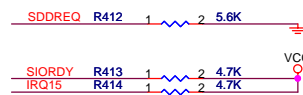
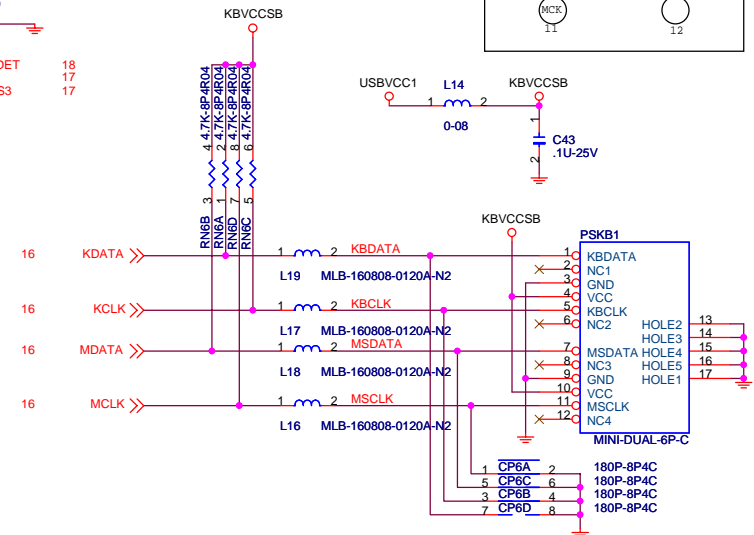
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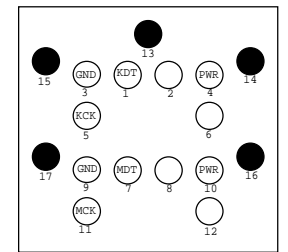
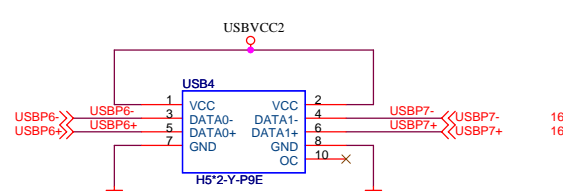
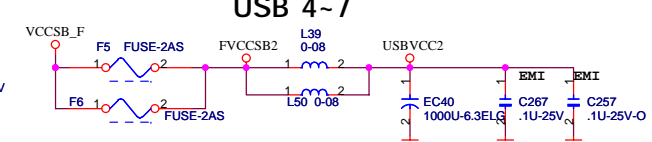




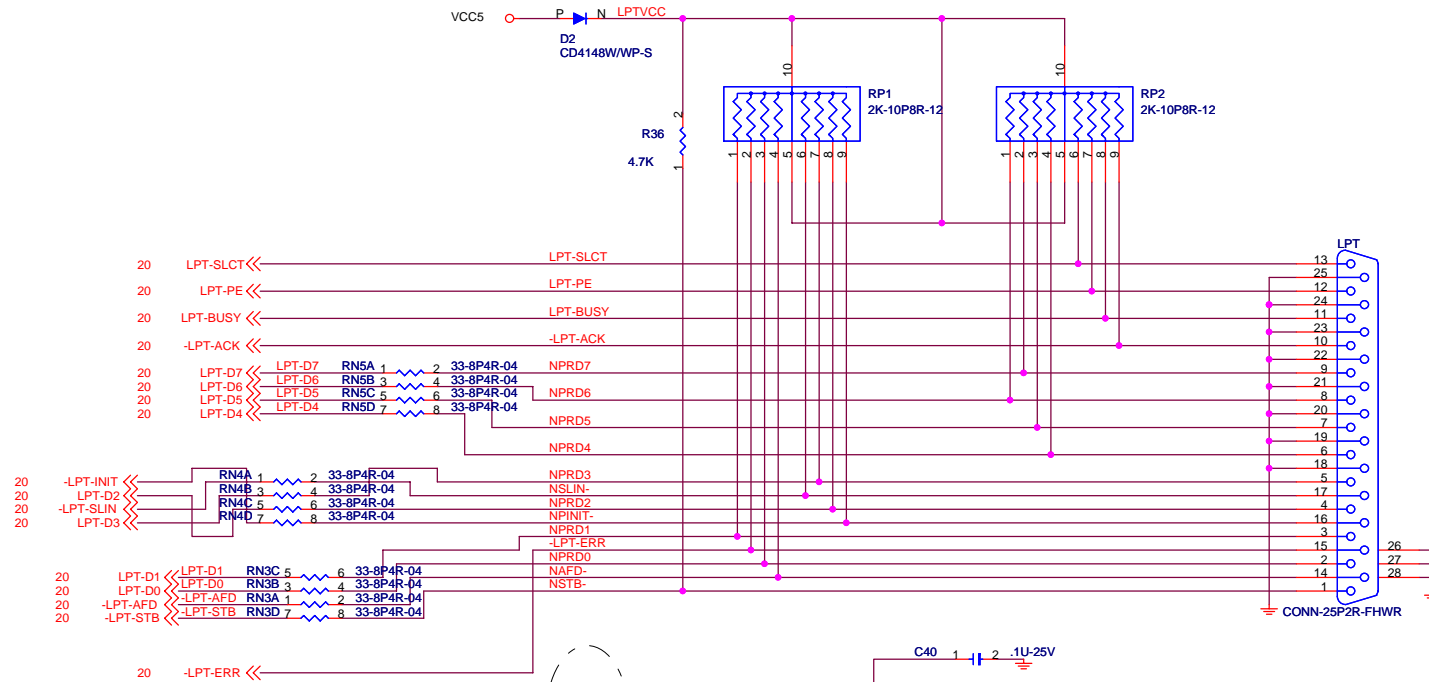




USB 4~7







Change VIN to +12VA 05/10/19

## CP1, CP2, CP3, CP4

LPT-SLCT	1	CP4A	2	180P-8P4C
LPT-PE	3	CP4B	4	180P-8P4C
LPT-BUSY	5	CP4C	6	180P-8P4C
-LPT-ACK	7	CP4D	8	180P-8P4C

NPRD7	1	CP3A	2	180P-8P4C
NPRD6	3	CP3B	4	180P-8P4C
NPRD5	5	CP3C	6	180P-8P4C
NPRD4	7	CP3D	8	180P-8P4C

NPRD3	1	CP2A	2	180P-8P4C
NSLIN	3	CP2B	4	180P-8P4C
NPRD2	5	CP2C	6	180P-8P4C
NPINIT	7	CP2D	8	180P-8P4C

NAFD	1	CP1A	2	180P-8P4C
NPRD0	3	CP1B	4	180P-8P4C
-LPT-ERR	5	CP1C	6	180P-8P4C
NPRD1	7	CP1D	8	180P-8P4C

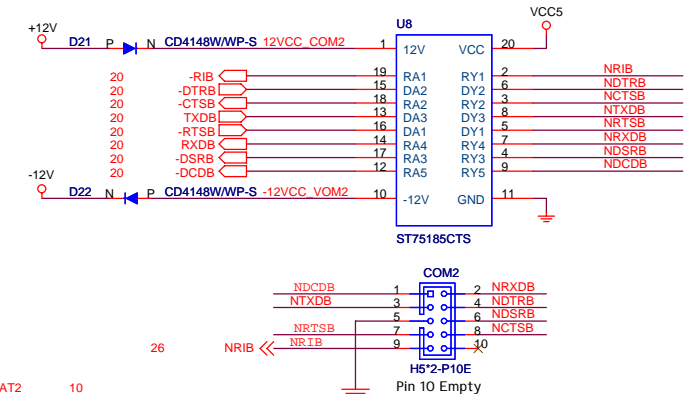
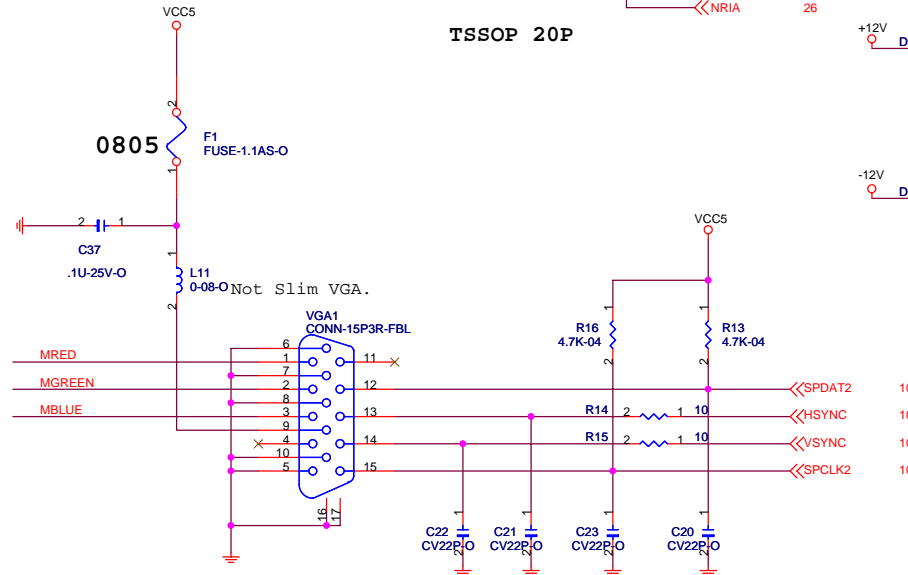
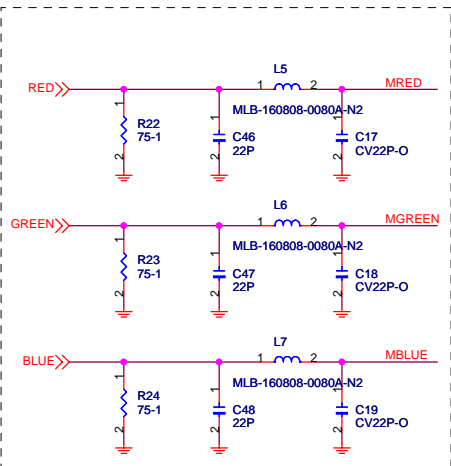
NSTB	1	C51	2	180P
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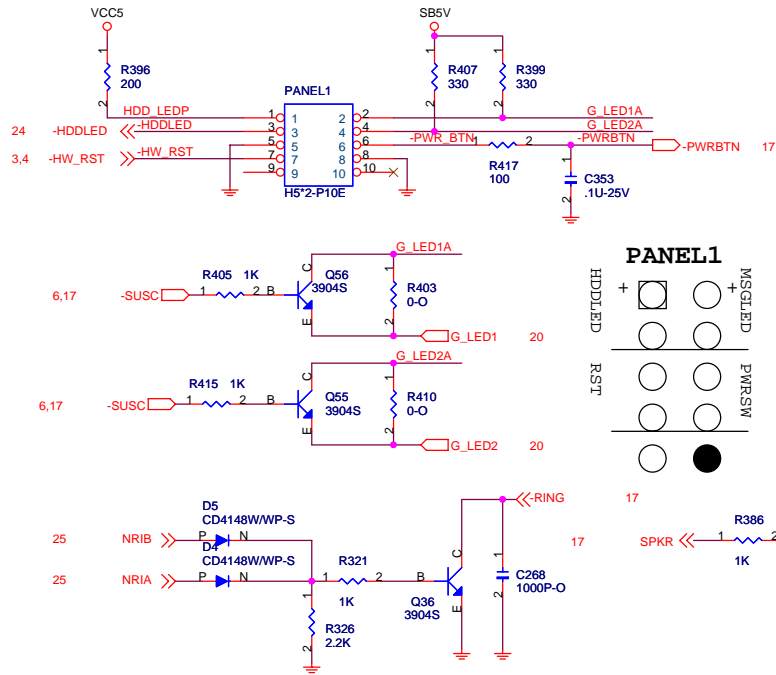
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NDSRA	3	CP5B	4	180P-8P4C
NRTSA	5	CP5C	6	180P-8P4C
NRTSA	7	CP5D	8	180P-8P4C

NDCDA	1	CP7A	2	180P-8P4C
NTXDA	3	CP7B	4	180P-8P4C
NRXDA	5	CP7C	6	180P-8P4C
NDTRA	7	CP7D	8	180P-8P4C

NDCDB	1	CP8A	2	180P-8P4C
NTXDB	3	CP8B	4	180P-8P4C
NRXDB	5	CP8C	6	180P-8P4C
NDTRB	7	CP8D	8	180P-8P4C

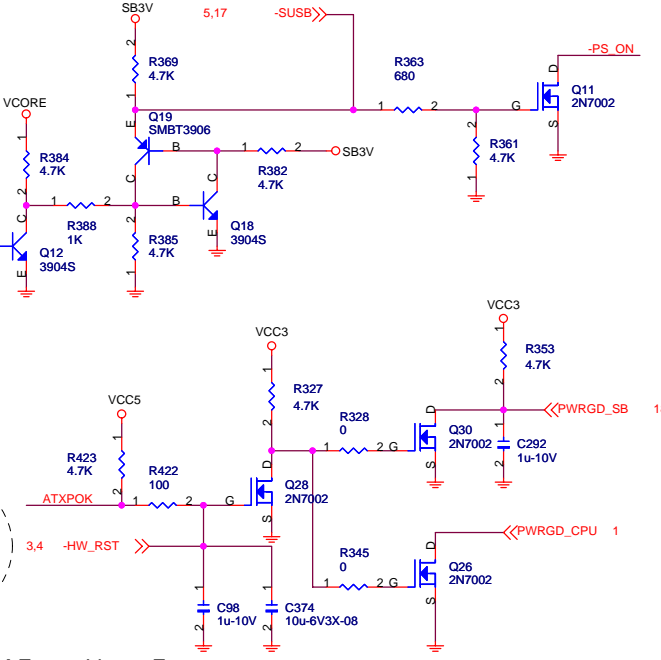
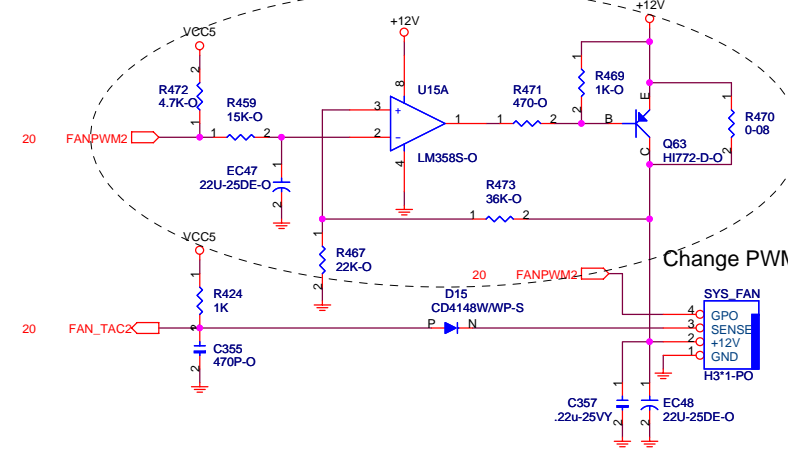
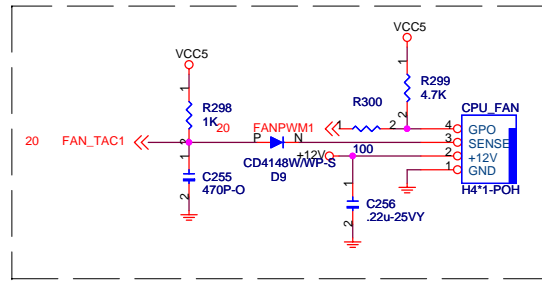
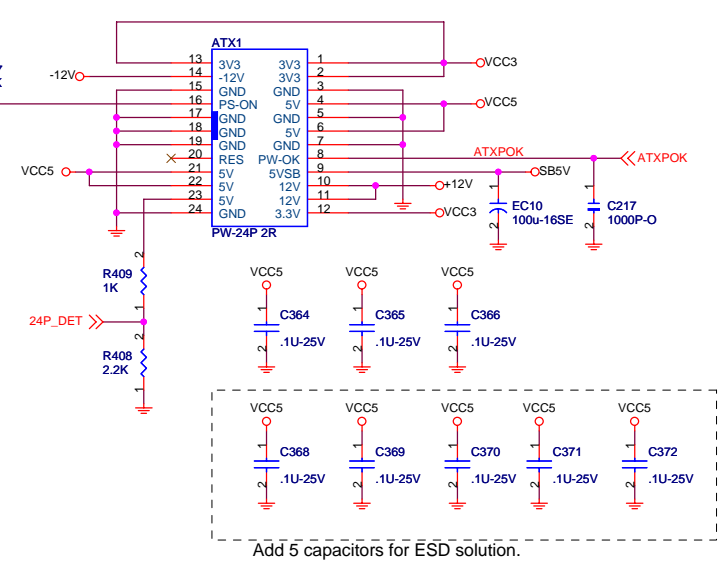
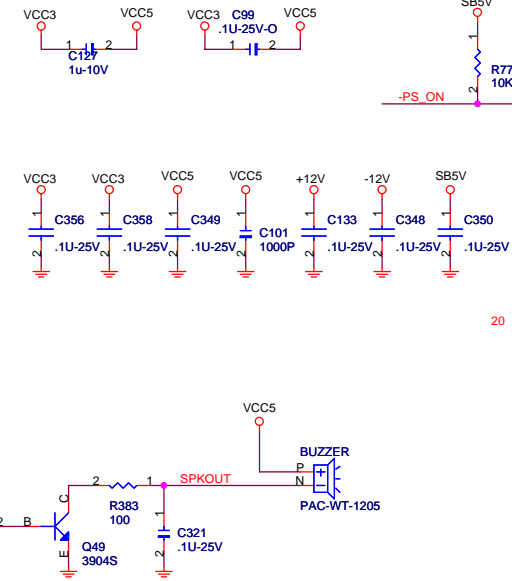
NRTSB	1	CP9A	2	180P-8P4C
NDSRB	3	CP9B	4	180P-8P4C
NRTSB	5	CP9C	6	180P-8P4C
NRTSB	7	CP9D	8	180P-8P4C

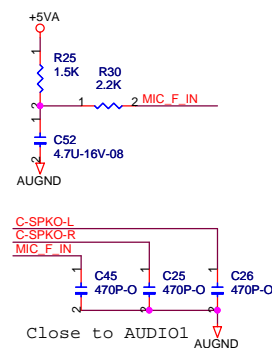
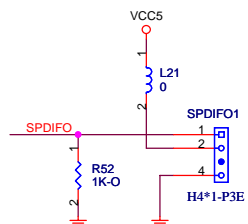
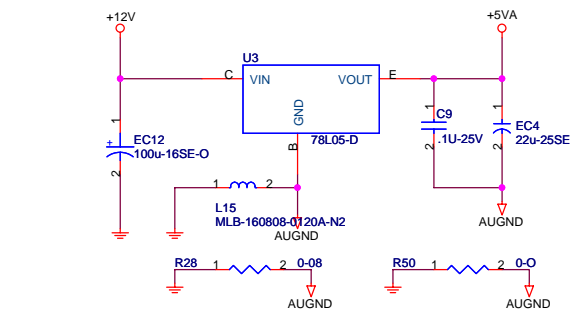
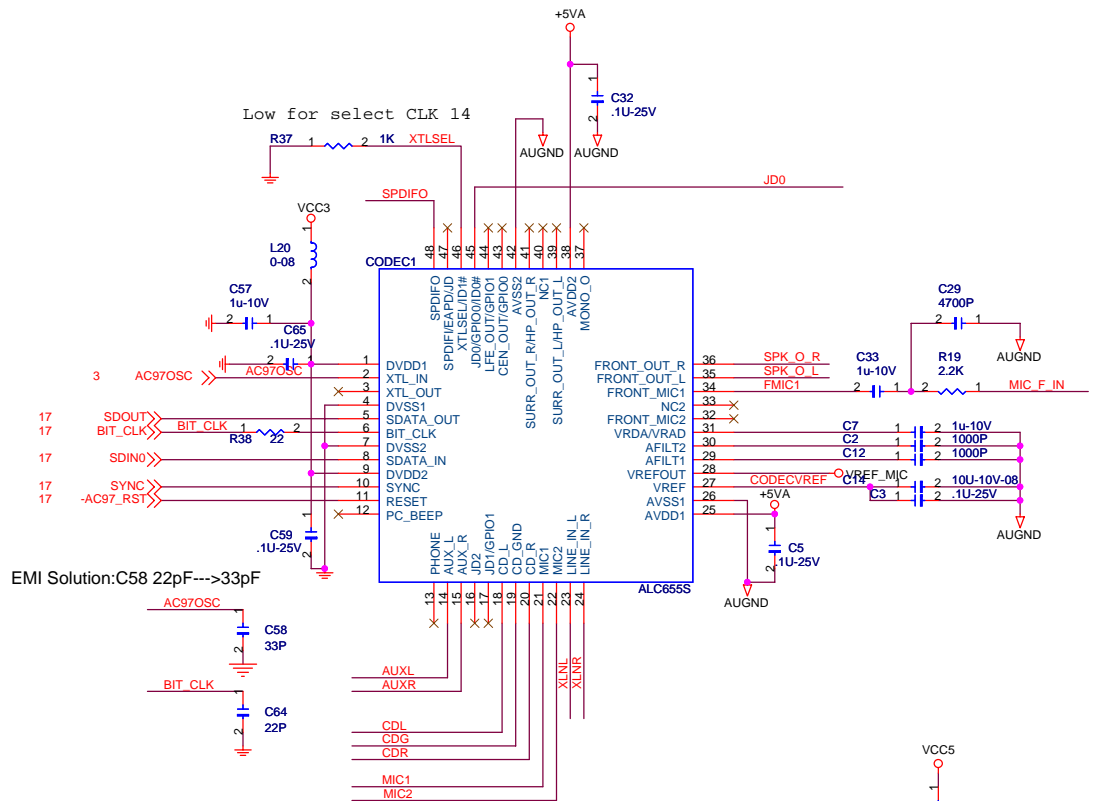




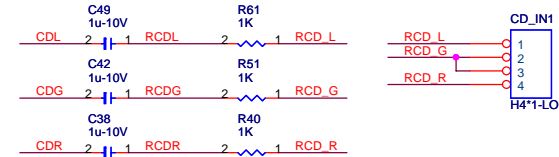
SUSST1#	SUSA#	SUSB#	SUSC#	MODE
0	0	0	0	Mechanical off
1	0	0	0	S4/S5
1	0	0	1	S3
1	0	1	1	S1
1	0	1	1	S0 (ON)

	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking Yellow	Dark
LSJ1(1,2)	Dark	Dark Blinking	Light	Dark
SJ1(1,3)(2,3)	Light		Blinking	Dark
GLD1	HIGH	HIGH	LOW	HIGH
GLD2	LOW	SWITCH	SWITCH	HIGH

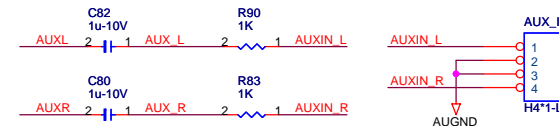




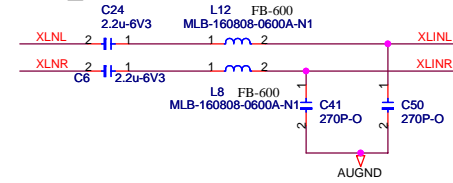
## CD-IN



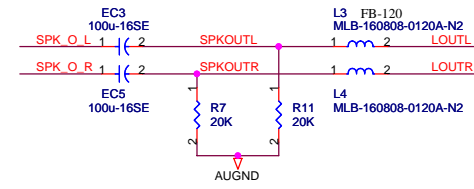
## AUX-IN



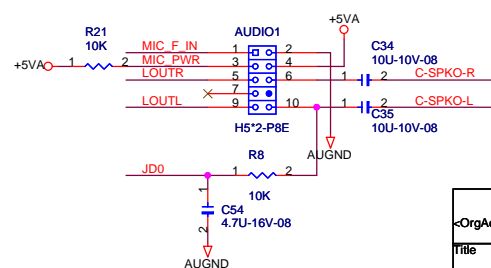
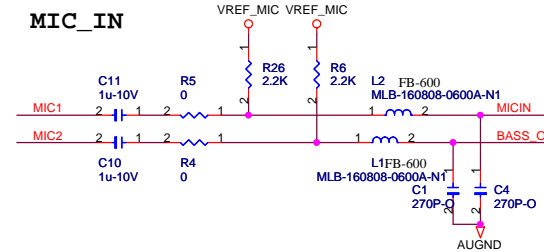
## LINE\_IN



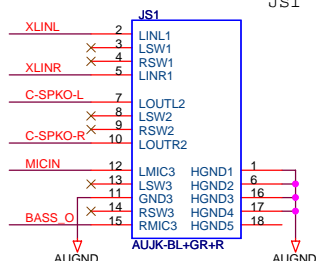
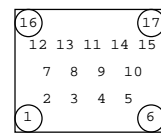
## LINE\_OUT



## MIC\_IN



## Top View



1	CPU P4-478(FSB)
2	CPU P4-478(PWR, GND)
3	Clock Generator
4	Power (CPU Vcore)
5	Power (DC to DC)
6	VDIMM & DDR VTT
7	NB P4M800pro (CPU)
8	NB P4M800pro (MEM)
9	NB P4M800pro (AGP, V-Link)
10	NB P4M800pro (VGA)
11	DDR II SLOT1
12	DDR II SLOT2
13	DDR I
14	DDR Terminator
15	AGP SLOT
16	SB 8237(PCI, USB)
17	SB 8237(IDE, GPIO, AC-Link)
18	SB 8237(V-Link, MII)
19	LAN PHY(VT6103L)
20	Super IO(ITE8705F GX)
21	PCI 1, 2
22	PCI 3
23	PCI LAN(RTL8100C)
24	USB, PS2, IDE
25	COM, LPT, VGA
26	Front Panel
27	AUDIO(ALC655), 6CH mute function
28	Cover Page
29	Block Diagram
30	Control table for BOM

# P4M800PRO-M478

**NO.1**  
P4M800PRO-M Revision information:

Rev : 1.0A 15-Q22-011000

Schematics	PCB Ver. 244*244*1.6 -2116	BOM	Schedule			
			Schematics	Layout	Gerber Out	M/B return
A	A	89-200-Q22000				
B	B	89-200-Q22010				
1.0	1.0	89-380-Q22100				
1.0A	1.0A					

L2:PWR      DDR Area L2:GND  
L3:GND      DDR Area L3:PWR

Rev:A Initial version:  
1. Base on P23G to modify placement and layout

Rev:B  
1. Schematic modify for DDR2 clock input to buffer .. etc  
2. Codec change to ALC655  
3. Del 1394 function  
4. Add RTL8100C PCI LAN optional

Rev:1.0  
1. Modify component lib.  
2. Modify LAN crystal placement

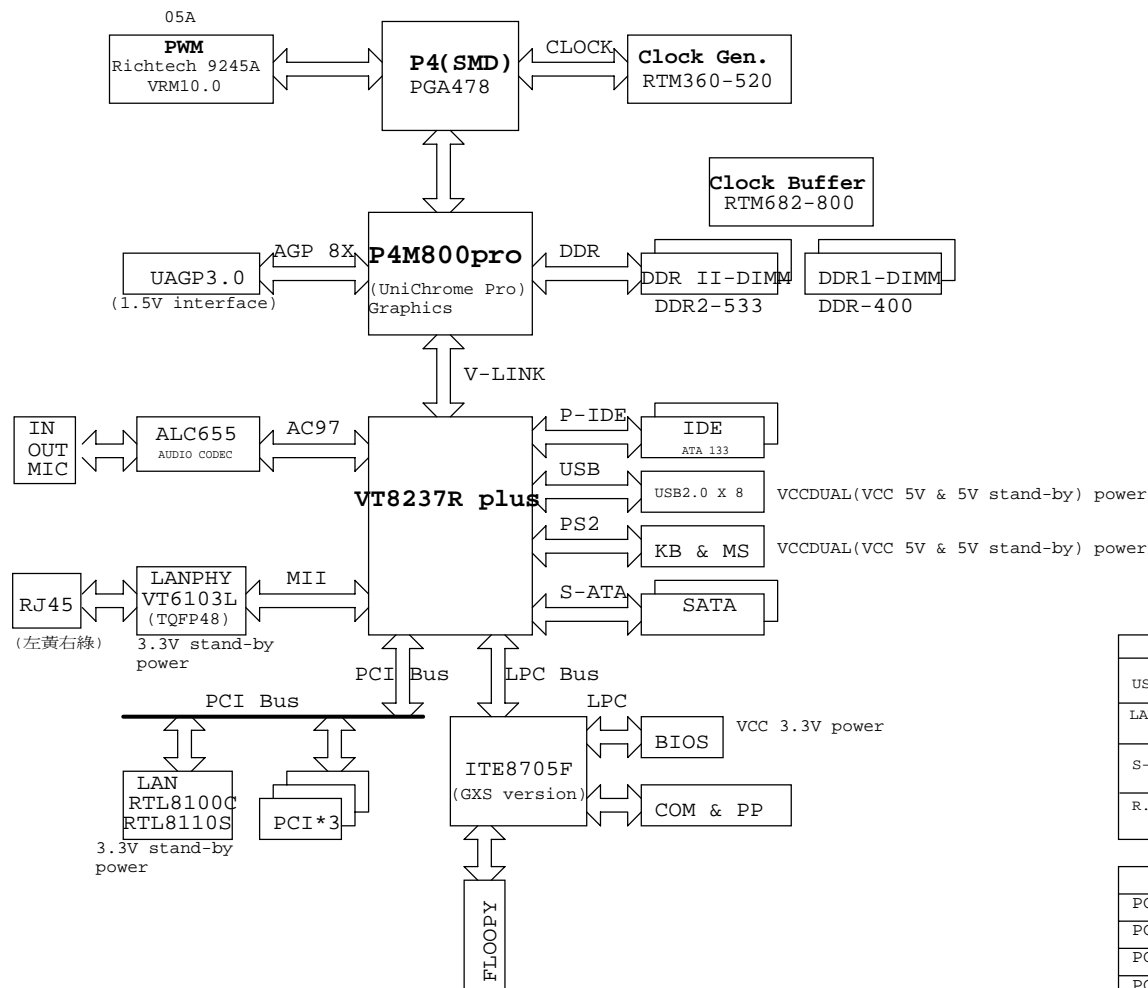
Rev:1.0A  
1. Modify ATX 24pin power conn. placemant by TF request

**NO.2**  
P4M800PRO-M478 Revision information:

Rev:A  
1.Base on P4M800PRO-M modify placement and layout  
2.Modify LAG775 CPU to PGA478.  
3.Modify CPU Vcore 4 phase to 3 phase,change RT9602CS to RT9603CS.

**NO.3**  
Rev:1.0  
1.Change RTL8100C to VT6103L(BOM Control)  
2.Cost down  
3.(W/WHQL)(BOM Control)  
4.Fix bug abuout CPU and reliability

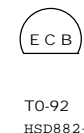
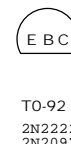
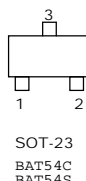
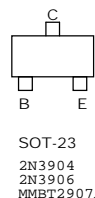
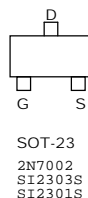
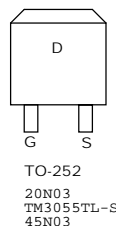
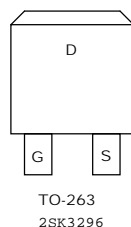
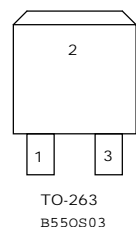
Elitegroup Computer Systems			
Title Cover Page			
Size Custom	Document Number P4M800PRO-M478		Rev 1.0
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	Impedance	PCB 2116
USB_DT0+/- (45/90)		8/8/8(47/87) 8/5/8(47/80 allegro) 7.5/7.5/7.5(50/90 guide)
LAN RX+/- TX+/- (50/100)		8/8/8(47/87) 8/12/8(47/91 guide)
S-ATA (50/100)		20/6/8/6/20(56/103) 17/6/8/6/17(guide) group mismatch 20 mil.
R.G.B (37.5)		50/10/10/10/10/10/50 12/?/12/?/12(guide) Put 75 ohm on CON

PCI Bus Resource			
PCI1	AD19	INTA,BCD	REQ0
PCI2	AD20	INTB,CDA	REQ1
PCI3	AD21	INTC,DAB	REQ2
PCI LAN	AD22	INTB	REQ3

22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm



Elitegroup Computer Systems			
Title Block Diagram			
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Control table for BOM

1,W/WHQL vs (W/WHQL)

Parts Location	W/WHQL	(W/WHQL)
Q41,Q42,Q44,Q60,R402,R406,R362,R366,R375 R460,R461,R72,R87,R85,R105,R62,R64 U12,U13,U5	V	X
R208,R210,R222,R228,R59,R68	X	V

PS:R68 for COM2 GPIO control.

2,Support VRD10 CPU Only(VA-->V1.0)

Delete:R268.  
Change to:R280-->47 OHM,R282-->680 OHM,C182,C183,C184-->X7R(04-007-105591),R192-->22K,R196-->150 OHM,R229-->NC,C202-->0.1uF,C212-->1000pF

3,Cost down(VA-->V1.0)

- 1>VCC12: Q53--> 2N7002-S,EC28-->C373 4.7u-08
- 2>VCORE: EC17,EC18,EC49,EC50,C174,C186,C187 Empty(BOM Control)
- 3>C199,C194,C188,C178,C173,C193,C197,C179,C195,C189 Empty(BOM Control) and change to SCXX(EX:C199-->SC199)
- 4>EC36,EC42,EC25,EC13,EC2 Empty(BOM Control)
- 5>F1,L11,C37,C17,C18,C19,C22,C21,C23,C20 Empty(BOM Control)
- 6>F2,F8--->0 OHM-0805. CHOKE2,CHOKE3--->0 OHM-0402
- 7>For SYS\_FAN:Del R472,R459,EC47,U15,R471,R469,Q63,R473,R467,EC48

4,Modify(VA-->V1.0)

- 1>C93,C97,C100 10pF-->22pF,R112,R117,R119, 20 OHM-->33 OHM,C140-->22pF.,C58 22pF-->33pF,R149 22 OHM-->33 OHM
- 2>ADD 5 bypass capacitors(0.1uF) to VCC5 for ESD solution. C368,C369,C370,C371,C372.
- 3>Add R133 1K-04 into BOM
- 4>Add C374 10uF(0805) for Founder solution

5,RTL8100C vs VT6103

	RTL8100C	VT6103L
R212,L45,L47,R462,R29,R213,C225,R48,R27,R49,R463,R464,R466,R465,R53,ECP2,R209,C232 R197 C16,C8,C359,C360,C216,C215,C205,C207,C204,Q5,Q15,L46,C210,Q10,L49,RN41,R198,R206	V	X
L13,C39,RN45,RN2,D19,D20,R20,R18,C31,R17,R12,R10,C28,R9,R91,R1,ECP1,C333,LAN1	X	V